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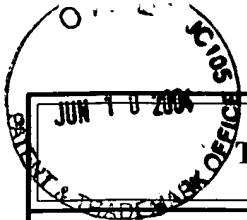
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AF 2827
IFW

JUN 10 2004

TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No.
MCT.0012D1US

In Re Application Of: **Salman Akram**

Serial No.
09/853,111

Filing Date
May 10, 2001

Examiner
Alonzo Chambliss

Group Art Unit
2827

Invention: **Method of Fabricating Mounted Multiple Semiconductor Dies in a Package (As Amended)**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on April 30, 2004.

The fee for filing this Appeal Brief is: **\$330.00**

- ☒ A check in the amount of the fee is enclosed.
- ☐ The Director has already been authorized to charge fees in this application to a Deposit Account.
- ☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

Signature

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Dated: **June 8, 2004**

I certify that this document and fee is being deposited on **June 8, 2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature of Person Mailing Correspondence

Cynthia L. Hayden

Typed or Printed Name of Person Mailing Correspondence

CC:



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:

Salman Akram

Serial No.: 09/853,111

Filed: May 10, 2001

For: Method of Fabricating Mounted
Multiple Semiconductor Dies in
a Package (as Amended)

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Art Unit: 2827

Examiner: Alonzo Chambliss

Atty Docket: MCT.0012D1US
97-0141.02

Mail Stop **Appeal Brief-Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed February 19, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

None.

06/14/2004 JADD01 00000105 09853111

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Date of Deposit: June 8, 2004

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Cynthia L. Hayden
Cynthia L. Hayden

III. STATUS OF THE CLAIMS

Claims 15-22, 32, 34, and 35 are rejected. Each rejection is appealed.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF THE INVENTION

Referring to Fig. 1, a semiconductor package 10A includes a first semiconductor die 20 and a second semiconductor die 30 stacked one on top of the other, and a leadframe 170 encapsulated by a package body 11. The package body 11 hermetically seals the first die 20, second die 30 and the leadframe 170 to protect the dies 20, 30 and the leadframe 170 from moisture and physical stress and mechanical damage. See specification at page 4, lines 18 through 29.

The first die 20, which may have a lead-on-chip (LOC) configuration, is mounted face down on the leadframe 170, with its face 21 adjacent a top surface 173 of the leadframe 170. The die 20 may be adhered to the leadframe 170 by an adhesive layer 160. The second die 30, which has a conventional configuration, is mounted face up on the first die 20, with its back 32 adjacent the back 22 of the first die 20, and adhered to the first die 20 by the adhesive layer 160. The adhesive layer 160 may be a nonconductive double adhesive tape such as the type conventionally used in LOC packages. Alternatively, a conductive adhesive layer can be used if a common electrical connection between the two die is required such as ground.

The leadframe 170 has leads 171 and lead fingers 172. The lead fingers 172 are encapsulated within the package body 11 and extend towards a center of the package body 11.

The leads 171 extend outside the package body 11 and may be formed into through-holes, J-leads, gull wings, or other variations thereof. To facilitate soldering of leads 171 to an interconnecting structure, leads 171 may be tin plated or solder dipped.

One advantage of the semiconductor device 10A is that multiple dies may be conveniently encapsulated in a single package body. Another advantage is that the multiple dies may have the same or may not have the same rectangular dimensions, even though both are shown as having the same dimensions in Figure 1. See specification at page 4, line 30 through page 5, line 31.

VI. ISSUES

A. Is Claim 15 Anticipated by Sota?

B. Is Claim 19 Anticipated by Sota?

VII. GROUPING OF THE CLAIMS

Claim 19 may not be grouped and all of the other claims may be grouped with claim 15 for convenience on appeal.

VIII. ARGUMENT

A. Is Claim 15 Anticipated by Sota?

The Examiner's argument that something can be in contact with something else through an intervening element makes no sense.

Claim 15 calls for a method for mounting multiple semiconductor dies on a single leadframe having fingers. The method includes stacking at least two semiconductor dies on top

of one another, such that one of the dies is mounted on top of the leadframe and the other said die is mounted on and in contact with the die mounted on the leadframe fingers.

The cited reference to Sota does not teach two dice “in contact” with one another. The Examiner’s position is apparently that something can be in contact with something else through an intervening element.

The Examiner suggests that “in contact” could include thermal or electrical communication. This argument is contrary to the well accepted dictionary definition. For example, Webster’s Collegiate Dictionary, 10th Edition, defines contact as the union or junction of surfaces. See definition attached.

The Examiner cites the embodiments of Figures 1 and 2 and assumes the claimed invention must be broad enough to cover both embodiments. There is no basis for this assumption.

In response to the question about whether or not an adhesive connection can be used, of course it can, but the problem is Sota does not merely show an adhesive connection. It shows a die 1 on the top of the leadframe and a die 1 on the bottom of the leadframe. The dice are on opposite sides of the leadframe 3, not both on top of it as called for by claim 15. The dice are separated not only by the resin 6 but, more significantly, by the leadframe 3 as well. Thus, under any conventional definition of “in contact,” the dice cannot be in contact.

The Examiner’s definition of “in contact” would simply put everything in contact with everything else in the universe, extending claims to a ridiculous extreme, and is completely without any support whatsoever.

Therefore, the rejection should be reversed.

B. Is Claim 19 Anticipated by Sota?

Claim 19 is dependent on claim 15 and calls for one of the dies to be secured to the leadframe and the other of said dies is secured to the die secured to the leadframe.

The final rejection suggests that one of the dies is the die 1 in Sota and the other of the dies secured to the die 1 by the die pad 2 "so that the die is secured to the leadframe."

However, in Sota, the two dies are secured on the opposite side of the leadframe and a die secured to the leadframe does not have another die secured to that die.

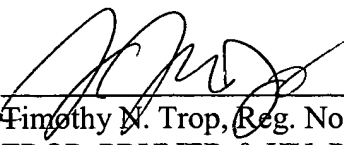
Therefore, the rejection of claim 19 should be reversed.

IX. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: June 8, 2004



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APPENDIX OF CLAIMS

The claims on appeal are:

15. A method for mounting multiple semiconductor dies on a single leadframe having fingers, comprising:

stacking at least two semiconductor dies having substantially the same rectangular dimensions on top of one another such that one of said dies is mounted on top of the leadframe fingers and the other of said dies is mounted on and in contact with the die mounted on the leadframe fingers; and

wirebonding each of said semiconductor dies to the same leadframe fingers.

16. The method of claim 15, wherein one of said semiconductor dies is mounted back to back on the other of said semiconductor dies.

17. The method of claim 16, wherein one of said semiconductor dies is adhered to the other of semiconductor dies by an adhesive layer.

18. The method of claim 15, wherein a first semiconductor die has a lead-on-chip configuration.

19. The method of claim 15, wherein one of said dies is secured to said leadframe and the other of said dies is secured to the die secured to the leadframe.

20. The method of claim 15, further comprising wirebonding the semiconductor dies to the leadframe, said dies having facing sides and outwardly facing sides by extending wires to bond pads on the outwardly facing sides of said die.

21. A method of connecting multiple semiconductor dies having bonding pads and a single leadframe having lead fingers, comprising:

locating a first semiconductor die on the lead fingers of the leadframe;

stacking a second semiconductor die on said first semiconductor die and in contact with said first semiconductor die; and

electrically connecting the bonding pads of the semiconductor dies to the same lead fingers of the leadframe.

22. The method of claim 21, further comprising encapsulating the semiconductor dies and the leadframe in a single package body.

32. A method for mounting multiple semiconductor dies on a single leadframe having fingers, comprising:

stacking first and second semiconductor dies having substantially the same rectangular dimensions on top of and in contact with one another;

mounting the first semiconductor die on a leadframe finger;

mounting the second semiconductor die on said first semiconductor die; and

wirebonding the first and second semiconductor dies to the same lead fingers of the leadframe.

34. The method of claim 32 wherein the first semiconductor die is mounted back to back on the second semiconductor die.

35. The method of claim 34 wherein the first semiconductor die is adhered to the second semiconductor die by an adhesive layer.



Merriam- Webster's Collegiate[®] Dictionary

TENTH EDITION

Merriam-Webster, Incorporated
Springfield, Massachusetts, U.S.A.

